UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,813	01/27/2004	Lakshmanan Ramakrishnan	15142US02	2449

23446   7590   03/17/2008
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER
WERNER, DAVID N

ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>24 December 2007</u>.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-5 and 7-20</u> is/are pending in the application.
    4a) Of the above claim(s) <u>1-4 and 13-15</u> is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>5,7-12 and 16-20</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on <u>24 December 2007</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
        1.☐ Certified copies of the priority documents have been received.
        2.☐ Certified copies of the priority documents have been received in Application No. _____.
        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

1.   This Office action for US Patent Application 10/765,813 is responsive to communications filed 24 December 2007, in reply to the Non-Final Rejection of 24 July 2004. Currently, claims 1-5 and 7-20 are pending. Of those, claims 1-4 and 13-15 have been withdrawn from consideration. Claim 6 has been canceled.

2.   In the previous Office action, claims 5, 9-12, and 20 were rejected under 35 U.S.C. 102(e) as anticipated by US Patent 7,007,031 B2 (MacInnis et al.). Claims 6-8 and 16-19 were rejected under 35 U.S.C. 103(a) as obvious over MacInnis et al. in view of US Patent 4,599,689 (Berman). The drawings were objected to on formalities. The specification was objected to on formalities. The title was objected to as not descriptive. Claim 5 was objected to on an informality.

Election/Restrictions

3.   Claims 1-4 and 13-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 24 December 2007.

4.   Applicant's election without traverse of claims 5-12 and 16-20 in the reply filed on 24 December 2007 is acknowledged.

Priority

5.   In a telephone conversation on 10 July 2007, Applicant's attorney stated that this application is related to application 10/735,980, now US Patent 7,284,072. A specific cross-reference to the prior-filed application must be included in the first sentence(s) of the specification following the title or in an application data sheet. See 37 CFR 1.78(a)(2)(i), "Cross references to other related applications may be made when appropriate".

Response to Arguments

6.   Applicant's arguments, see page 1, filed 24 December 2007, with respect to the rejection(s) of claim(s) 5-8 and 16-19 under 35 U.S.C. 103(a) as obvious over MacInnis et al. in view of Berman have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as US Patent 7,007,031 B2 (MacInnis et al.) at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. Since MacInnis et al. only qualifies as prior art under 35 U.S.C. 102(e), it is disqualified as prior art under 35 U.S.C. 103(c). However, upon further consideration, a new ground(s) of rejection is made in view US Patent 6,178,203 B1 (Lempel).

7.   Applicant's arguments filed with respect to claims 9-12 and 20 under 35 U.S.C. 102(e) have been fully considered but they are not persuasive. Applicant argues that MacInnis does not teach the claimed limitation of "transmitting an indicator to a direct

memory access engine indicating that the local buffer can store another portion of the video data".

In the prior Office action, bridge module 204 of MacInnis et al. was mapped to the claimed "extractor" of claims 9 and 20 of the present invention. The bridge module 204 moves data between decoder memory 212, mapped to the claimed "local buffer" in claims 9 and 20 of the present invention, and main memory 110 (column 6: lines 46-51). The bridge module, however, acts according to instructions from core processor 202, and forms part of a data unit processing pipeline (column 6: lines 10-14). In the pipeline, after data in a buffer is decoded and transferred to its destination (in this example, macroblock 0,0), the buffer is free (column 11: line 63–column 12: line 7). Then, the next available macroblock (in the example, macroblock 0,5) is transferred into the buffer to start processing. This pipeline is controlled by core processor 202 (column 12: lines 46-54). Then, a fetch command to read data from main memory 110 via bridge module 204 (column 6: lines 10-14) corresponds with the claimed indicator, since this only may be sent when a buffer is available to take in new data in the pipelined data processing unit. Therefore, the examiner respectfully maintains that every feature of claims 9 and 20 is taught by MacInnis.

Drawings

8.   Replacement drawings were received on 24 December 2007. These drawings are acceptable.

Specification

9.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

The following title is suggested: "Automatic Direct Memory Access Engine and

Method for Dual Macroblock Row Transfer in a Video Decoder".

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11.   Claims 9-12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by

US Patent 7,007,031 B2 (MacInnis et al.).

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art

under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the

invention "by another," or by an appropriate showing under 37 CFR 1.131.

MacInnis et al. discloses a memory system and a pipeline for a video decoder. Regarding claim 9, figure 2 of MacInnis et al. illustrates a media decoding system that can be used as a video decoder (column 5, lines 20-22). Decoder memory 212 locally stores a data unit containing macroblock information received from main memory (column 6, lines 1-14). This corresponds with the claimed "local buffer". When decoding system 200 acts as a video decoder, core processor 202, co-processor 206, and accelerators 208 and 210 comprise a chipset that performs picture decoding and decompressing (column 6, lines 15-20). Each component uses decoder memory 212 as a local memory (column 6, lines 52-64). Then, decoder 200 corresponds with the claimed "decompression engine". Bridge module 204 communicates with the local decoder memory 212 and main memory 110, according to instructions from core processor 202 (column 6, lines 46-51). This corresponds with the claimed "extractor". The bridge module acts to fetch data from main memory 110 into a pipelined data processing system including local decoder memory 212 (column 6: lines 4-14) when a buffer memory is free (column 11: line 63–column 12: line 7). Then, the fetch instruction corresponds with the claimed "indicator".

Regarding claim 10, as shown in figure 1 of MacInnis et al., DMA controller 106 controls data transfer between system memory 110 and a local memory in video decoder 116 (column 4, lines 57-64). Then, when core processor 202 in video decoder 116 issues a command to read from system memory 110 to local memory 212 through bridge module 204, it inherently does so through DMA controller 106.

Regarding claim 11, core processor 202 acts to direct a pipeline, individually receiving and processing macroblocks one at a time and storing them in local memory 212. The local memory, in turn, contains a plurality of buffers that each store information for one macroblock between operations (column 7, lines 20-41). In the illustrative example described throughout MacInnis et al., five buffers each store macroblock data during processing. When a buffer becomes free, core processor 202 stores a new macroblock to continue decoding (column 16, lines 15-35).

Regarding claim 12, as mentioned previously, local memory 212 contains a plurality of buffers, each of which can store data for a different macroblock simultaneously, and co-processor 206 contains two separate units that can simultaneously decode different macroblocks (column 13, lines 26-35).

Regarding claim 20, digital media system 100 of MacInnis et al. corresponds with the claimed "decoder system", digital video decoder 116 corresponds with the claimed "video decoder", decoder memory 212 corresponds with the claimed "local buffer", bridge 204 corresponds with the claimed "extractor", and DMA controller 106 corresponds with the claimed "direct memory access engine".

Claim Rejections - 35 USC § 103

12.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13.   Claims 5, 7, 8, and 16-19 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,178,203 B1 (Lempel) in view of US Patent 4,599,689 (Berman). Lempel teaches a system for decoding two rows of MPEG2 bitstream video data at the same time. Regarding claim 5, figure 6 of Lempel shows the process of decoding two macroblock rows: a "top row" and a "bottom row". First, at step 602, the leftmost macroblock in the first row of a video in a cache memory (column 5: lines 1-2). This occurs when a variable length decoding unit detects an MPEG2 start slice code (column 3: lines 60-67; column 4: lines 38-46). The detection of a slice start code corresponds with the claimed "request" for a macroblock row. Next, at step 604, the leftmost macroblock in a next row of video is stored (column 5: lines 3-5), and at step 606, the macroblock in the top row is decoded (column 5: lines 5-7). Macroblocks in both rows continue to be alternatively stored and decoded (column 5: lines 8-29) until the end of a macroblock row is reached. This process corresponds with the claimed steps of providing successive portions of the two macroblock rows and checking if a previous portion of each row has been decoded. When Lempel reaches the end of the row, it retrieves pointers to the beginnings of the next two rows and decodes those rows. However, while Lempel discusses pointers to macroblock row beginnings, it does not disclose particulars of how the memory is addressed.

Berman teaches a Direct Memory Address (DMA) control apparatus. Regarding claim 5, in the invention of Berman, to transfer data from a main memory through a DMA, a processor first stores the starting address of the data in the main memory in a current address register in the DMA (column 5, lines 42-46). In a system in which the

data is loaded from two multiple locations, in this case, two buffers (column 8, lines 30-36), the start address for each buffer is loaded (column 8, lines 56-58).

Lempel discloses the claimed invention except for details of memory addressing. Berman teaches that it was known to increment an address in a DMA controller during a sequential data transfer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the DMA control system of Berman into the decoder of Lempel, as taught by Berman, since Berman states in column 1, lines 33-59 that such a modification would enable a system to automatically handle a large amount of data transfer from a memory while the main processor performs other operations.

Regarding claims 7 and 8, in Berman, the DMA engine loads a word count, specifying the number of words to be transferred from a memory, with the starting address (column 9, lines 3-20). Data is then sequentially transferred word by word, and the address register and word counter are incremented (column 6, lines 12-14). This sequential transfer of data corresponds with the claimed "providing successive portions".

Regarding claim 16, the system of Berman may be incorporated in the variable length decoding module 22 of Lempel. In this case, the two locations of the macroblock rows in the off chip whole-frame buffer of Lempel (column 4: lines 25-30) correspond with the two memory addresses in Berman. Regarding claim 17, in Berman, the two starting addresses are stored in registers (column 6, line 5; column 8, lines 56-58).

Regarding claims 18 and 19, as mentioned previously, the DMA control apparatus of Berman increments the address registers one word at a time and provides data for a specified word count.

Conclusion

14.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,892,522 A (Moutin) teaches a system for addressing memory in an MPEG decoder, in which macroblocks are divided into half-blocks of odd lines and even lines. US Patent 6,658,056 B1 (Duruöz et al.) teaches an MPEG-2 video decoder that decodes video data one macroblock row at a time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner, whose telephone number is (571)272-9662. The examiner can normally be reached on MWF from 9:00-6:30, TR from 9:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri, can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. N. W./
Examiner, Art Unit 2621

/Mehrdad Dastouri/
Supervisory Patent Examiner, Art Unit 2621